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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,933	11/26/2003	Asif Q. Khan	4-14-28	9641

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EXAMINER	
O CONNOR, BRIAN T	
ART UNIT	**PAPER NUMBER**
2616	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,933	KHAN ET AL.	
	Examiner	Art Unit	
	Brian T. O'Connor	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/26/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because the abstract contains more than 150 words; according to 37 CFR 1.72 (b) the abstract may not exceed 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Objections

2. Claim 20 is objected to because of the following informalities: claim 20, on line 6, recites "the first and second tables", however no tables are mentioned previous to line 6. Appropriate correction is required.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claim 20 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 20 recites "a machine-readable storage medium"; this is viewed as non-statutory subject matter due to the claim's lack of including a computer compatible medium so that the method can be combined and executed on a computer. Amendments to the claims to recite a "computer-readable medium" would overcome this rejection. The Examiner also suggests the Applicant review the "Interim Guidelines for Statutory Subject Matter" published in the Official Gazette on November 22, 2005.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anconetani et al. (US 7,120,153; hereafter Anconetani).

With respect to claims 1 and 19, Anconetani discloses a method and processor (72 of Figure 7; 72, 102 of Figure 10) for transferring ATM data cells between an ATM network (12 of Figure 7) and a PSTN class-4 or class-5 switch (78 of Figure 7). The processor includes scheduling circuits (204, 208 of Figure 11) to schedule the ATM data cells for transmission from a from of virtual circuits (VC1, VC2 of Figure 7) or telephone port modules (76 of Figure 7) and conducts the scheduling by using a calendar table (206 of Figure 11; viewed as a first table) and a context table (202 of Figure 11; viewed as a second table). Also present in the processor is a memory module (210 of Figure 11) provided to support the scheduling and store parts of calendar table.

The calendar table is build from calendar entries (Figure 11; viewed as a first list of entries) and calendar bins (Figure 11; viewed as a second list of entries) related to virtual circuits that produce the ATM data cells (column 9, lines 26-46). The table has an array of link lists, one of ordinary skill in the art would recognize this array of lists as a table pointer, used to track a conformance time for transmitting at a determined rate

(column 9, lines 16-22). Cells with different ATM service contracts have differing priorities for transmission (column 9, lines 29-31).

The context table has a group of entries for each VC (column 9, lines 48-55) and schedules ATM data cells according to minimum period for a connection and leaky bucket state in the calendar table (column 9, lines 50-55; viewed as a different scheduling algorithm from the calendar table). The context table will decide when to transmit a cell (column 10, lines 4-8) based on a scheduling period or rate (Tpcr; column 9, line 64 – column 10, line 3).

Anconetani does not disclose any context table pointer used to identify a current entry as being ready for transmission.

Office Notice is taken that both the practice and benefit of using pointers with memory for implementing an algorithm are well known and expected in the art. It would have been obvious to use pointers to identify the packets ready for transmission in the table of Anconetani as the use of pointers is known to provide smaller and faster algorithm execution in the memory of devices.

With respect to claim 2, Anconetani further discloses the calendar table used a group of FIFO lists (210 of Figure 11) and an array of link lists (column 9, lines 16-22)

With respect to claim 3, Anconetani further discloses the calendar table has an array of link lists, one of ordinary skill in the art would recognize this array of lists as a table pointer, used to track a conformance time for transmitting at a determined rate (column 9, lines 16-22; viewed as identifying the lists as active)

With respect to claim 4, Anconetani further discloses the scheduling algorithm looks through the calendar entries and calendar bins for ATM data cells to transmit and once found the cell is evaluated for conformance and then set as ready to transmit (column 9, lines 25-36).

With respect to claim 5, Anconetani further discloses placing cells in en-queue or de-queue processes depending on the leaky bucket state and TPCR (column 11, lines 49-66; viewed as creating an active list and a pending list and TPCR is viewed as a programmable time interval).

With respect to claim 6, Anconetani further discloses that when a cell en-queue process has finished all its cells it is then switched to a cell de-queue process (column 13, lines 36-40).

With respect to claim 7, Anconetani further discloses that the context table will keep track of cells based upon TPCR (column 9, line 64 – column 10, line 3).

With respect to claim 8, Anconetani further discloses that the context table has multiple slots (202 of Figure 11).

With respect to claim 9, Anconetani further discloses that the processor runs on a finite timer (column 12, lines 27-32) and that the state of ATM data cells is updated based on the progression of the timer.

With respect to claim 10, Anconetani further discloses that each VC held in the context table can have a separate TPCR for transmission rates (column 9, lines 48-52).

With respect to claim 11, Anconetani further discloses that the context table can hold a leaky bucket state for each VC that is evaluated periodically and that the

context table also holds a separate TPCR for transmission rates (column 9, lines 48-52).

With respect to claim 12, Anconetani further discloses that TPCRs are programmable (column 12, lines 33-40; where the TPCR is set to a maximum to stop the leaky bucket logic).

With respect to claim 13, Anconetani further discloses that a data block moves through the scheduler and is not in a calendar table and a context table at the same time (Figure 14).

With respect to claim 14, Anconetani further discloses a round robin service for the scheduler (column 11, lines 32-37).

With respect to claim 15, Anconetani further discloses a constant bit rate scheduling algorithm (column 9, lines 15-22) and that the context table will control when a cell is ready for transmission thereby controlling a bit rate.

With respect to claim 16, Anconetani further discloses that the memory (210 of Figure 11) is internal memory.

With respect to claim 17, Anconetani further discloses data packets or ATM cells as data blocks (column 7, lines 45-48).

With respect to claim 18, Anconetani further discloses a network processor integrated circuit (ATM Ingress Port of Figure 10) to move data between an ATM network (12 of Figure 7) and a PSTN class-4 or class-5 switch (78 of Figure 7).

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anconetani and further in view of Kumar et al. (US 7,085,279 hereafter Kumar).

With respect to claim 20, Anconetani discloses a method using a processor (72 of Figure 7; 72, 102 of Figure 10) for transferring ATM data cells between an ATM network (12 of Figure 7) and a PSTN class-4 or class-5 switch (78 of Figure 7). The processor includes scheduling circuits (204, 208 of Figure 11) to schedule the ATM data cells for transmission from a from of virtual circuits (VC1, VC2 of Figure 7) or telephone port modules (76 of Figure 7) and conducts the scheduling by using a calendar table (206 of Figure 11; viewed as a first table) and a context table (202 of Figure 11; viewed as a second table). Also present in the processor is a memory module (210 of Figure 11) provided to support the scheduling and store parts of calendar table.

The calendar table is build from calendar entries (Figure 11; viewed as a first list of entries) and calendar bins (Figure 11; viewed as a second list of entries) related to virtual circuits that produce the ATM data cells (column 9, lines 26-46). The table has an array of link lists, one of ordinary skill in the art would recognize this array of lists as a table pointer, used to track a conformance time for transmitting at a determined rate (column 9, lines 16-22). Cells with different ATM service contracts have differing priorities for transmission (column 9, lines 29-31).

The context table has a group of entries for each VC (column 9, lines 48-55) and schedules ATM data cells according to minimum period for a connection and leaky bucket state in the calendar table (column 9, lines 50-55; viewed as a different scheduling algorithm from the calendar table). The context table will decide when to

transmit a cell (column 10, lines 4-8) based on a scheduling period or rate (Tpcr; column 9, line 64 – column 10, line 3).

Anconetani does not disclose a context table pointer used to identify a current entry as being ready for transmission.

Office Notice is taken that both the practice and benefit of using pointers with memory for implementing an algorithm are well known and expected in the art. It would have been obvious to use pointers to identify the packets ready for transmission in the table of Anconetani as the use of pointers is known to provide smaller and faster algorithm execution in the memory of devices.

However, Anconetani fails to disclose a machine-readable medium for storing a software programs.

Kumar, in the same field of endeavor, discloses a computer readable medium storing a program to perform a connection setup over a packet network in conjunction with a switching network. The computer-readable medium is an electronic, magnetic, optical, or other physical device or means that can be contain or store a computer program for use by or in connection with a computer-related system or method (column 7, lines 51-67). One skilled in the art would have clearly recognized that the method of Anconetani would have been implemented in a software module. The implemented software would perform the function with less expense and more flexibility. Therefore, it would have been obvious to have use the technique in Anconetani as is and implement it as taught by Kumar in order to reduce cost and improve the adaptability and flexibility of the networking system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. O'Connor whose telephone number is 571-270-1081. The examiner can normally be reached on 9:00AM-6:30PM, M-F, 1st Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brian T. O'Connor
August 14, 2007

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